IN THE SPECIFICATION:

Page 5, please replace the paragraph starting at line 13 with the following amended paragraph:

Between the input and output pin rows 12 and ~~39~~ 36, the chip has a memory cell array. Horizontal digit lines are orthogonal to vertical word lines to define sixteen (16) cell plates 62. The cell plates 62 are arranged in two cell columns 64 and 66. The two cell columns 64 and 66 are disposed between the input and output pin rows 12 and 36. Each of the cell columns 64 and 66 includes four (4) pairs of cell plates 62.

Page 6, please replace the paragraph starting at line 21 with the following amended paragraph:

The ATD pulse synthesizer 90 is disposed within a central area of the chip and thus generally equally distant from the row 88 and the output pin row 36. The output circuitry 92 is disposed within an area nearest to the ~~outer~~ output pin row 36

Page 8, please replace the paragraph starting at line 1 with the following amended paragraph:

With reference to Figure 2, another embodiment of a semiconductor memory device is now designated by the reference numeral 100. The memory device 100 is substantially

the same as the memory device 10 except the location of an output circuitry 92. In the memory device 100, the output circuitry 92 is disposed in a row 102 between cell columns 64, 66 and an output pin row 36.

Page 8, please replace the paragraph starting at line 8 with the following amended paragraph:

With reference to Figure 3, another embodiment of a semiconductor memory device is now designated by the reference numeral 110. The memory device ~~100~~ 110 is substantially the same as the memory device 10 except the provision of an error correction code (ECC) circuitry 112. The ECC circuitry 112 is disposed in a column 94 between two amplifier columns 72, 74 together with an ATD pulse synthesizer 90. A delay circuitry 86 provides an ECC data latch signal also in response to the output from the ATD pulse synthesizer 90 as will be readily understood from the signal-timing diagram in Figure 7. This signal-timing diagram is substantially the same as that in Figure 6 except that the synthesized pulse fed to the delay circuitry 86 provides an ECC data latch signal also.

Page 8, please replace the paragraph starting at line 21 with the following amended paragraph:

With reference to Figure 4, another embodiment of a semiconductor memory device is designated by the reference numeral 120. The memory device 120 is substantially the same as the memory device 110 except the location of an output circuitry 92. In the memory device ~~100~~ 120, the

output circuitry 92 is disposed in a row 102 between cell columns 64, 66 and an output pin row 36.